

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-19 are pending in the present application with Claims 1-4 and 11 having been amended by the present amendment.

In the outstanding Office Action, Claims 1 and 11 were rejected under 35 U.S.C. § 112, first paragraph; and Claims 1-19 were objected to, but were otherwise indicated as allowable.

Regarding the rejection of Claims 1 and 11 under 35 U.S.C. § 112, first paragraph, the outstanding Office Action indicates there is no support for the negative limitation “without bonding wires.” In light of this indication, Claims 1 and 11 have been amended to remove this phrase. Rather, Claim 1 has been amended to recite that the first and second main surfaces of the at least one semiconductor chip are electrically connected to the predetermined two power terminals by soldering or pressure welding. Claim 11 recites similar features. These features are described in original Claim 4, and at page 9, lines 7-19 and page 16, beginning at line 6.

Further, in the previous outstanding Office Action mailed April 2, 2003, the outstanding Office Action stated Matsuda teaches the claimed invention. However, as shown in Figure 2, the first and second main surfaces of the transistor 29 or diode 31 (i.e., the top and bottom surfaces) are not sandwiched between and in parallel with a predetermined two power terminals such that the first and second main surfaces are electrically connected to the predetermined two power terminals by soldering or pressure welding. Rather, the top surfaces (i.e., main surface of the chips) are connected to the power terminals via Al bonding wires 35.

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Further, it is respectfully submitted the side surfaces of the transistors 29 are not equivalent to first and second main surfaces as claimed by the present invention. Thus, the first and second surfaces in Matsuda are not sandwiched between and in parallel with the terminals, but rather the side surfaces are between two terminals. In addition, as shown in Figure 2, the top surface of the transistor 29 is connected to the power terminal via the bonding wires 35.

Accordingly, it is respectfully submitted independent Claims 1 and 11 and each of the claims depending therefrom are allowable.

In addition, it is respectfully requested this amendment be entered as the feature brought into the independent claims has already been examined. Thus, no new issues have been raised.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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